UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,290	08/26/2003	Masanori Kinugasa	241976US2	2662

22850 7590 09/22/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,290	KINUGASA ET AL.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,5,6,9,12,15,16,20 and 21* is/are allowed.

6)☒ Claim(s) *3,4,7,8,10,11,13,14 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08262004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figures 8-9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. [Pages 1 (lines 19-21) and 6 (lines 8-9) both identify Fig. 8 as a "conventional analog switch", and pages 3 (line 35) and 6 (lines 10-12) relate Fig. 9 to Fig. 8.] See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "3" and "C1" of Fig. 3; and "VGP" and VGN" of Figs. 1, 3-4, and 6-9. However, it is believed "substrate 10" on line 11 of page 8 (with respect to the description of Fig. 3) should recite --substrate 3-- because "10" is actually the bus switch circuit shown in Fig. 5. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include

all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 3, line 24 "o" should be --to--. Page 8, line 19 "lever" should be --level--. Page 9, lines 1-7 need clarification. As presently written, it appears that when a high voltage is supplied to both terminals I/O and O/I the signal transmission is cut off. However, is this because both the input and output terminals are both at the same voltage (i.e. a voltage higher than the power supply voltage), or because P1 and N1 are actually turned off (i.e. made none conducting)? Page 10, lines 16-17 are misleading and/or inaccurate. Although the lines indicate "diodes D1-D6 are composed of MOS transistors M1-M6", Fig. 4 shows only diode configured MOS transistors M1-M4 in place of diodes D1-D4 (shown in Fig. 1). Diodes D5-D6 are still shown in Fig. 4 with the common diode symbol. Appropriate corrections are required.

Claim Objections

Claims 5-8, 11, 13-14, 17, and 19 are objected to because of the following informalities: To minimize possible confusion, it is suggested --first-- be added prior to "transistor" on line 4 of claim 5. Since the power supply terminal had been previously recited within claim 1, it is

suggested that "a" be changed to either --the-- or --said-- on line 7 of claim 7. For similar reasons, it is suggested "a" on both lines 4 and 8 of claim 8 be changed to either --the-- or --said-- because claim 1 has already identified the source and drain terminals of the first transistor. Line 3 of both claims 11 and 19 should have "a gate voltage" changed to clearly refer back to "a gate voltage" in claims 1 (line 12) and 12 (line 10), respectively. Claims 13 (line 6) and 17 (line 7) "a power" should be changed to relate back to "a power supply terminal" recited in claim 12 (line 21). Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-4, 7-8, 10-11, 13-14, and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is understood ordinal numbers indicate order or sequence. Therefore, the use of "a third rectifying element" in claim 3 (line 3) implies a second that is not identified within the claim's chain of dependency. Was the second element meant to be initially recited within claim 1 (e.g. see claims 10 and 11, which also appear to imply the second element has already been identified). Although claim 4 actually indicates the first and third rectifying elements are formed on the second region, it is not clear in claim 3 how "a semiconductor region" on line 7 relates to the "second semiconductor region" of claim 1 (lines 17-18). The use of "a fourth rectifying element" in claims 7 and 17, and the use of "a fifth rectifying element" in claims 8 and 18, imply at least one other element (e.g. a second rectifying

element) that is not identified within each claim's respective chain of dependency. Claim 13 has the same type of problem as claim 3 with respect to how "a semiconductor region" of the third rectifying element relates to the second semiconductor region. Each of claims 8 and 18 recites the limitation "said second transistor" in line 11 with insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "said first and second rectifying elements" in line 2. Although a first element has been previously identified, there is insufficient antecedent basis for the second element limitation in the claim.

Each of claims 11 and 19 recites the limitation "said second transistor" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites the limitation "the substrate of said first transistor" in both lines 5 and 9 with insufficient antecedent basis for this limitation in the claim. Does this limitation actually refer back to the "back gate of said first transistor" recited within claim 12? If so, consistent labeling would minimize possible confusion.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Allowable Subject Matter

Claims 1-2, 5-6, 9, 12, 15-16, and 20-21 are allowed. Although various prior art references show and disclose a switch circuit comprising a first transistor, a control circuit, and at least one rectifying element, there is presently no strong motivation to modify or combine any prior art reference(s) to ensure that the following limitations are met: 1) the first transistor is formed in a first semiconductor region, separate from a second semiconductor region which includes a first rectifying element, as recited within claims 1 (upon which claims 2, 5-6, and 9

depend), and 20; and 2) the first/second rectifying elements, formed in first/second semiconductor regions, as recited within claims 12 (upon which claims 15-16 depend) and 21.

Also, claims 3-4, 7-8, 10-11, 13-14, and 17-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. These claims depend on their respective independent claim 1 or 12, which are allowed as described above.

Prior Art

The prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Of special interest is Williams. Each of Figs. 15-17B clearly shows a switch circuit comprising first/second terminals; a first transistor coupled between first/second terminals; a control circuit; and at least four rectifying elements. For example, Fig. 15 shows first transistor 1500 coupled between first/second terminals X/Y; control circuit 1510,1520 for controlling gate voltage Vg of first transistor 1500; and rectifying elements D3 and D4, wherein D3 is coupled between first terminal X and power supply terminal V_{in} of the control circuit, and D4 is coupled between second terminal Y and power supply terminal V_{in}. However, the reference does not clearly show or disclose first transistor 1500 being formed in a first semiconductor region, and a first rectifying element (e.g. D3) being formed in a second semiconductor region separate from the first semiconductor region. Fig. 6 of Heminger et al. shows first transistor 38 coupled between first/second terminals V_{IN}/V_{OUT}; control circuit 40,58 which controls a gate voltage of first transistor 38; and first rectifying element 56. However, element 56 is coupled between first terminal V_{IN} and the same line of control circuit 40,58 that provides the gate voltage to 38, wherein it is understood from the applicants' disclosure and

figures that the control voltage and power supply terminal of the control circuit are actually two separate connections. Also, although Fig. 8 of Heminger et al. shows sections 98 and 104, which correspond to Fig. 6's 56 and 38, respectively, and column 6, lines 38-40 indicate 98 and 104 are isolated by ILD 90, "90" is not clearly identified in Fig. 8, nor does the reference provide a clear (reason) why the transistor and element would be formed in separate regions. Fig. 1 of Shimoda discloses first transistor 3, and rectifying element 8 coupled between first terminal 1 and power supply terminal 12 of control circuit 10. However, this reference also does not clearly show or disclose the first transistor being formed in a first semiconductor region while the rectifying element is formed in a second semiconductor region separate from the first.

The prior art references cited on the IDS submitted Aug 26, 2003 were reviewed and considered. All three of these references show CMOS type switch circuits comprising first/second transistors of opposite conductivity, and a control circuit for providing gate voltages to those transistors. However, references AB and AC do not show or disclose a rectifying element (e.g. diode). Reference AA is considered the most relevant to the claimed invention. Using Fig. 1 as an example, other than the lack of a (parasitic) rectifying element (i.e. diode) coupled between first terminal IN1 and the back gate of first transistor P1, block 504 of the figure corresponds to the conventional analog switch shown in the applicants' own Fig. 8. However, this reference also does not clearly show or disclose a rectifying element coupled between first terminal IN1 and the power supply terminal of control circuit NAND1,INV5.

One of ordinary skill in the art knows a transistor and rectifying element can be formed in the same region (e.g. see transistor P, (parasitic) diodes D5-D6, and diode D1 shown in the applicants' own conventional Figs. 8-9, wherein it is understood transistor P1 and rectifying

element D1 are both formed in region NW). Therefore, there is presently no strong motivation to ensure the transistor and diode are formed in separate regions.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

9 September 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800